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Clean Version of Pending Claims

VOLTAGE-LEVEL CONVERTER
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1. (Amended) A voltage-level converter comprising:

a static voltage-level converter including an inverter coupled to no more than two transistors in the static voltage-level converter; and

a split-level output circuit coupled to the static voltage-level converter.

2. (Amended) The voltage-level converter of claim 1, wherein the static voltage-level converter comprises:

an input node, a first output node, and a second output node;

a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to the input node;

a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node, wherein the inverter is coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node.

3. The voltage level converter of claim 2, wherein the split-level output circuit comprises a plurality of insulated-gate field-effect transistors.

4. The voltage-level converter of claim 1, wherein the static voltage-level converter comprises a first output node and a second output node and the split-level output circuit comprises a first split-level input node, a second split-level input node, a split-level output node,

a first insulated-gate field-effect transistor (FET) coupled to the first split-level input node and a second insulated-gate FET coupled to the second split-level input node, the first insulated-gate FET being connected in series with the second insulated-gate FET, the first insulated gate FET and the second insulated gate FET having a common node coupled to the split-level output node and the first split-level input node coupled to the first output node and the second split-level input node coupled to the second output node.

5. The voltage-level converter of claim 4, wherein the first insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect transistor.

6. The voltage-level converter of claim 5, wherein the second insulated-gate field-effect transistor comprises an n-type insulated gate field-effect transistor.

29. The voltage-level converter of claim 1, wherein the static voltage-level converter includes two down-sized transistors.

30. The voltage-level converter of claim 29, wherein the two down-sized transistors are insulated gate field-effect transistors.

31. The voltage level converter of claim 2, wherein the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are down-sized.

32. The voltage level converter of claim 32, wherein the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are insulated gate field-effect transistors.